PHENIX Silicon Vertex Tracker (VTX)

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Abstract

This technical note contains a report on the PHENIX Silicon Vertex Tracker (Pixel and Stripixel Trackers), including detailed information on the detector hardware and readout electronics.

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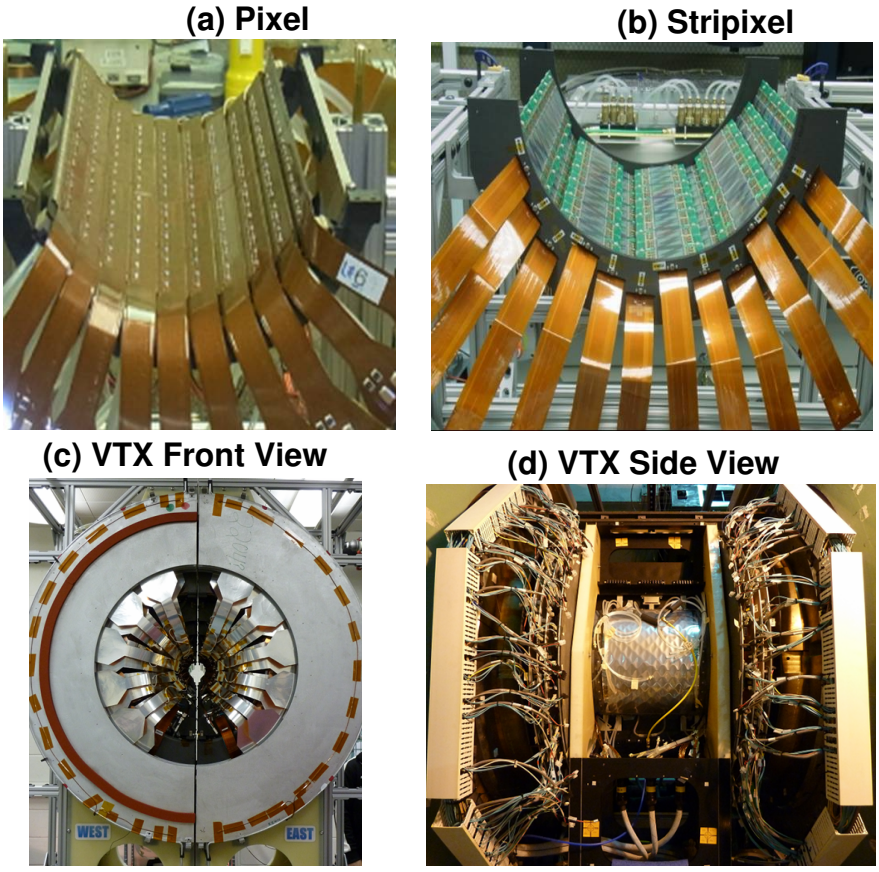

Figure 1: Panel (a) half barrel of the silicon pixel tracker, panel (b) half barrel of the silicon stripixel tracker, panel (c) front view of the VTX tracker (VTX closed position), and panel (d) side view of the VTX.

1 Overview

The RHIC upgrade with a luminosity increase for Au+Au, and for polarized proton beams motivated the PHENIX experiment upgrade to exploit with an enhanced detector new physics then in reach. For this purpose, we constructed the Silicon Vertex Tracker (VTX). The VTX detector has the tool to measure new physics observables that are not accessible at RHIC or available only with very limited accuracy. These include a precise determination of the charm production cross section and transverse momentum spectra-particularly high-p_T a measurement of beauty and charm. As shown in figure 1, the VTX consisted of four layers of barrel detectors located in the region of pseudorapidity $|\eta| < 1.2$ and covered almost 2π azimuthal angle. The inner two silicon barrels consisted of silicon pixel sensors and their technology is the ALICE1LHCb sensor-readout hybrid, which was developed at CERN for the ALICE and LHCb experiments. The outer two barrels consisted of silicon stripixel tracker with a new "spiral" design, single-sided sensor with 2-dimensional (X-U) read-out. In the following sections, we will present technical descriptions of the VTX tracker (VTX tracker = silicon pixel tracker (two barrels) + silicon stripixel tracker (two barrels), respectively. The VTX tracker collected data at RHIC in proton-proton collisions and the high multiplicity environment of heavy-ion collisions, like Au+Au at $\sqrt{s_{NN}} = 200$ GeV as well in small collisions systems at different energies.

2 VTX Silicon Pixel Tracker

In the PHENIX experiment at RHIC, the Silicon Pixel Tracker consists of two layers of barrel detectors and approximately 22 cm long, covers almost 2π azimuth angle, and pseudorapidity range $|\eta| < 1.2$. The first barrel, with a radius of 2.5 cm, is built from **10 pixel ladders**, while the second barrel is built from

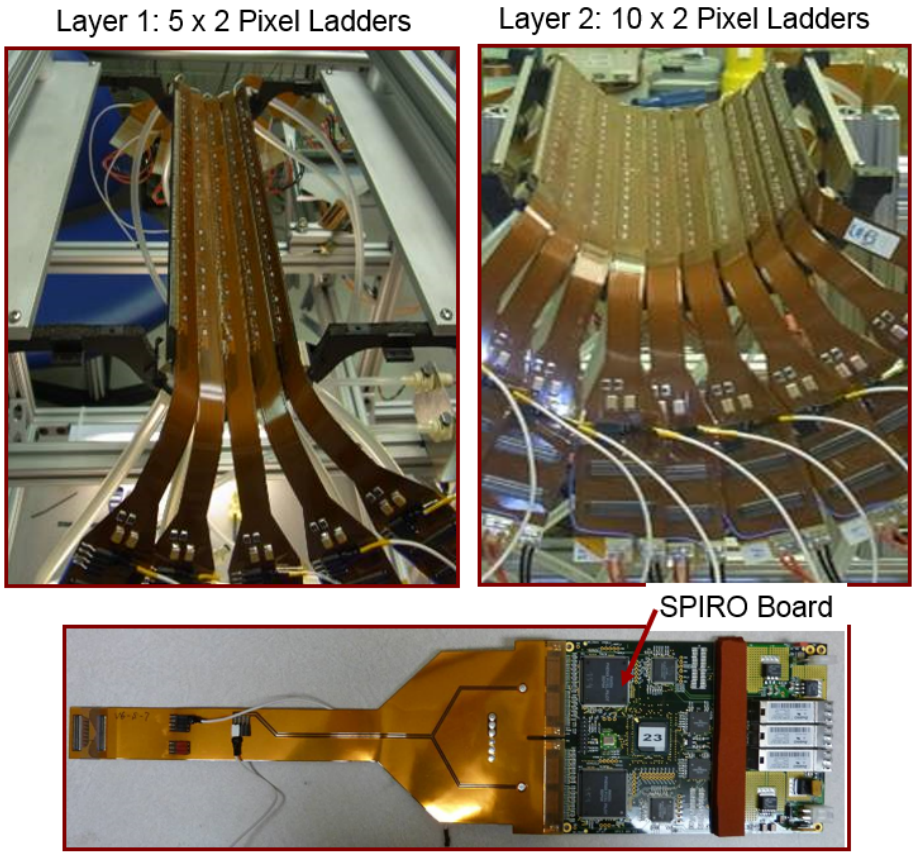

Figure 2: View of half silicon pixel barrels (layers 1 and 2). Bottom picture shows the pixel ladder connected to the SPIRO readout board.

20 pixel ladders with a radius of 5 cm, shown in the Fig. 2. The summary of physical specifications of Silicon Pixel Tracker are summarized in Table 1. The specifications have been chosen so that the design has a low material budget to avoid tracks being randomly bent by multiple scattering, and to minimize photon conversion ($\gamma \rightarrow e^+e^-$) which generates a background for electron identification in outer detectors.

2.1 Readout System

The readout system for the Silicone Pixel Tracker is divided into 60 sub-systems; each sub-system consists of one half ladder as shown in Fig.3.

A half **pixel ladder** consists of two pixel sensors with four bump-bonded readout chips respectively. Each readout chip handles 256 rows $\times$ 32 columns of data. The sensors and readout chips used in the silicone pixel tracker detector were originally developed for the ALICE experiment. The data is read out through four 32 bit buses in the half-ladder by the Silicon Pixel Read-Out (SPIRO) board. The SPIRO board receives the data and sends it to the FEM (Front-End Module) via optical links. The FEM receives the data from SPIRO board and sends it to the PHENIX DAQ system. It also provides clock, trigger and slow control to the SPIRO boards.

2.1.1 Pixels Ladder

Each pixels ladder is electrically divided into two independent half-ladders which are mounted on a carbon composite stave. The stave provides both mechanical support and cooling for the ladder. Each half-ladder consists of two **sensor modules** wire-bonded to a multi-layer readout bus (pixel bus) and is connected by a flexible bus extender to a Silicon Pixel Read-Out (SPIRO) module. The SPIRO module provides all

VTX		Pixel Detector	
	Layer	R1 (B0)	R2 (B1)
Geometrical dimensions	R (cm)	2.6	5.1
	Δz (cm)	21.8	21.8
	Area (cm^2)	280	560
Channel count	Sensor size R $\times$ z(cm^2)	1.28 $\times$ 1.36 (256 $\times$ 32 pixels)	
	Channel Size	50 $\times$ 425 μm^2	
	Sensor/ladder	4 $\times$ 4	
	Ladders	10	20
	Sensors	40	80
	Readout chips	160	320
	Readout channels	1,310,720	2,621,440
Radiation length (X/X$_0$)	Sensor	0.21 %	
	Readout chip	0.16 %	
	Bus	0.22 %	
	Support and cooling	0.67 %	
	Total	1.26 %	
Occupancy	Au+Au at 200 GeV	0.53%	0.16 %

Table 1: Summary of physical specifications of silicon pixels tracker

voltages, control and timing signals while also reading out the pixel data for a half ladder. The SPIRO module is connected via optical fibers to the pixel Front End Module (FEM) which is the trackers interface to the PHENIX data acquisition system (DAQ).

2.1.2 Sensor Module

Each sensor module consists of a silicon pixel sensor bump-bonded with four ALICE1LHCb **readout chips**. The pixel sensor are designed in the planar technology of CANABERRA and produced as $p-$in$-n$ structures on 5" silicon wafers of 200 μm thickness. The **pixel cell** dimensions are 425 μm $\times$ 50 μm, with each cell having a contact pad for bump-bonding to the readout chip. Each sensor contains four 32 $\times$ 256 pixel arrays in a linear arrangement on a single substrate. The depletion voltage for the 200 μm thick sensors is typically 12 volts. Pictures of silicon pixel module, pixel readout chip and the structure of half-ladder are presented in figure 4. a), b) and c), respectively.

2.1.3 Readout Chip

In this section, we present some technical details on pixel cell because it is crucial to understand the pixel cell functionality and how to mask or activate a pixel (threshold for a pixel). The readout chip, the ALICE1LHCb, is a mixed analog- digital ASIC designed by the CERN EP-MIC group for the ALICE and LHCb experiments [3, 4]. The chip is fabricated in a commercial 0.25 μm CMOS process using 6 metal layers. This offers the advantages of high component density and intrinsic radiation tolerance due to the thin gate oxide of the transistors. The radiation tolerance is further enhanced by the use of enclosed gates for the NMOS transistors to minimize drain-to-source leakage, and guard rings to prevent inter-component leakage and reduce the risk of electrically- or radiation-induced latch- up. The library and the design techniques of the readout-chips guarantee the radiation hardness of the chip up to 30 kRads (for more details see Ref. [5]). All the configuration registers in the chip have been designed to improve their immunity to single-event-upset. Both the analog and digital circuitry operate with a 1.8 V power supply,

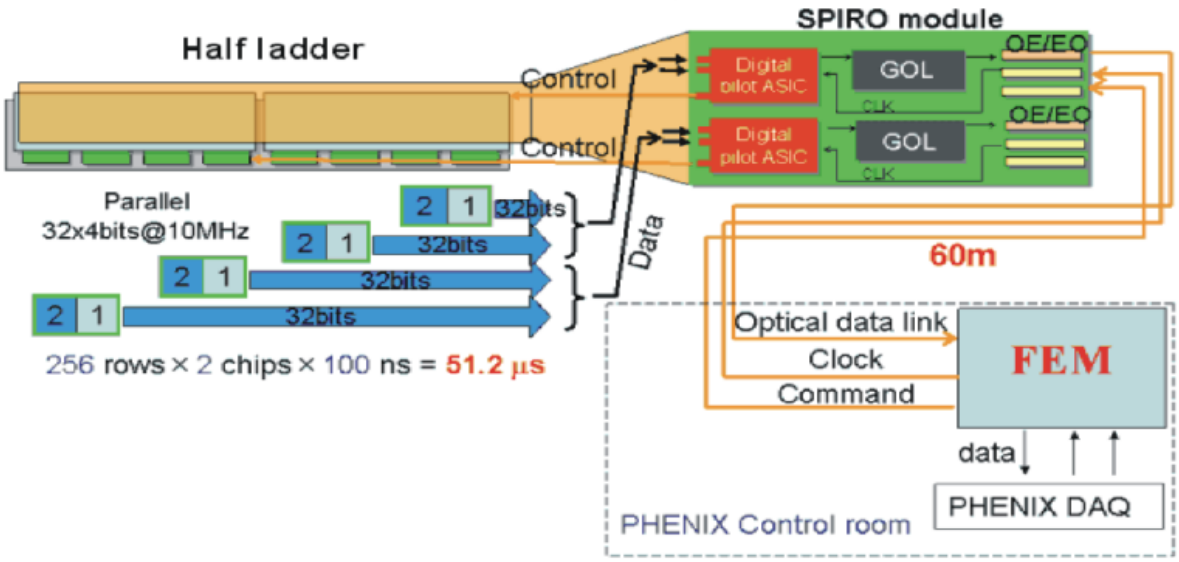

Figure 3: Pixel detector readout scheme

and the total power consumption is 800 mW. Each chip, the sensitive area measures 13.6 mm x 12.8 mm, and is divided into 8192 **pixel cells** of 425 μm (z) $\times$ 50 μm (ϕ). These pixels are arranged in 256 rows and 32 columns. The remainder of the chip consists of peripheral control logic, biasing circuitry, a JTAG serial interface and the input/output blocks, giving a total chip size of 14 mm $\times$ 15 mm. The chip contains around 13 million transistors.

The pixel cell is divided into an analog and a digital sections, as shown in the schematic of Fig. 5. The analog front-end is described in detail in [6]. An important feature is the use of a differential pre-amplifier and shaper to improve the common-mode rejection of the circuitry and to minimize the sensitivity to digital switching noise injected into the front-end through the substrate. A test input can be given to the pre-amplifier using a voltage step applied across a capacitor. The step is generated by a circuit in the chip, triggered by an external logic pulse, and transmitted to all the pixels. A discriminator compares the output of the shaper with a threshold fixed globally across the chip. In addition, each pixel contains three logic bits which can be used to adjust finely the thresholds on a pixel-to-pixel basis. The discriminator output is fed into the digital part of the cell, described in detail in [7]. The first stage consists of two digital delay units, whose purpose is to store a hit for the duration of the trigger latency. The result of the trigger coincidence is loaded into the next-available cell of a 4-event FIFO, which acts as a multi-event buffer and de-randomiser. Data is read out by means of a flip-flop which forms one element of a column shift register. One feature of note is the use of current-starved logic to reduce the injection of switching noise from the digital circuitry into the sensitive analog front-end. Finally, there are five latches inside the cell whose contents switch on or off the test input to the front-end, mask or activate a pixel, and provide the three bits of threshold adjustment.

As we mentioned before each chip is divided into 8192 **pixel cells**. Data for each chip is read out on a 32-bit wide data bus at 10 MHz, allowing all data from a single readout chip to be read out in 25.6 μsec. Four readout chips are bump-bonded on a single sensor chip with microscopic solder balls of 20 μm. This is called sensor module. The size of a sensor module is 15.6 mm $\times$ 57 mm and total thickness is 380 μm approximately, see Figure 4. a) and b). Each half-ladder is made of two sensor modules. The two sensor modules of one half-ladder are wire-bonded to a **readout bus** made of Copper-Aluminum-Polyimide Flexible Printed Circuit board (FPC). The readout bus is connected to a Silicon Pixel Interface ReadOut (SPIRO) board which controls the readout chips, reads out and transfers the binary pixel data to the PHENIX DAQ system via 1.6 Gbit/sec optical links.

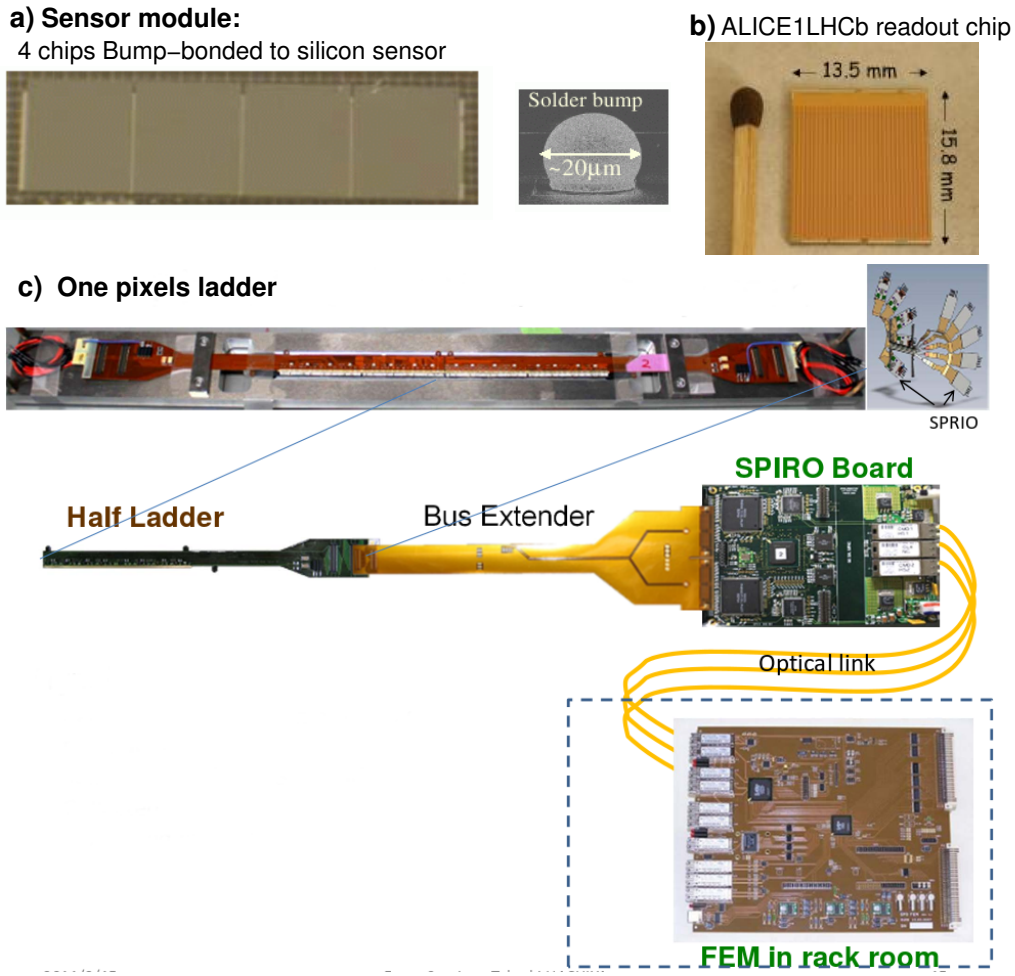

Figure 4: Panels a), b) and c) show a picture of a silicon pixel sensor, a picture ALICE1LHCb readout chip and a picture of assembled half pixel ladder with its readout chain, respectively

2.1.4 Readout Bus

The VTX collaboration have developed a new high density readout bus for the Pixel Detector. It is a Copper-Aluminum-Polyimide Flexible Printed Circuit board (FPC). There are two requirements that the readout bus must satisfy: it can read-out the system in $\sim$ 50 μsec and it must fit in the small space in the VTX tracker.

- It takes 25.6 μsec to read-out one ALICE1LHCb chip at 10 MHz with a 32-bit data width. Thus in order to achieve the detector readout time of $\sim$ 50 μsec, two of the four ALICE1LHCb readout chips in a sensor hybrid should be read out in parallel simultaneously. There are two sensor hybrids on a half-ladder that is read-out by a single bus. This means that the bus should read out four ALICE1LHCb readout chips simultaneously.

- To avoid mechanical conflict with the neighboring ladder, the on-detector, part of the pixel readout bus (the first $\sim$ 15 cm length) must fit within the width of the sensor hybrid itself, i.e. 1.4 cm.

- To minimize the multiple scattering and photon conversion, the thickness of the bus, in terms of radiation length, should be as small as practical. The allowed thickness was $<$ 500 μm.

- The total length of the bus, from the farthest sensor hybrid to the SPRIO read-out board, is $\sim$ 60 cm.

- To make and handle the bus easily, the bus must be flexible.

In order to realize the system as described above, the development of a high signal density bus was essential. The bus has a total of 188 lines, 128 data and 60 control, and it fit within the 14 mm width of the sensor

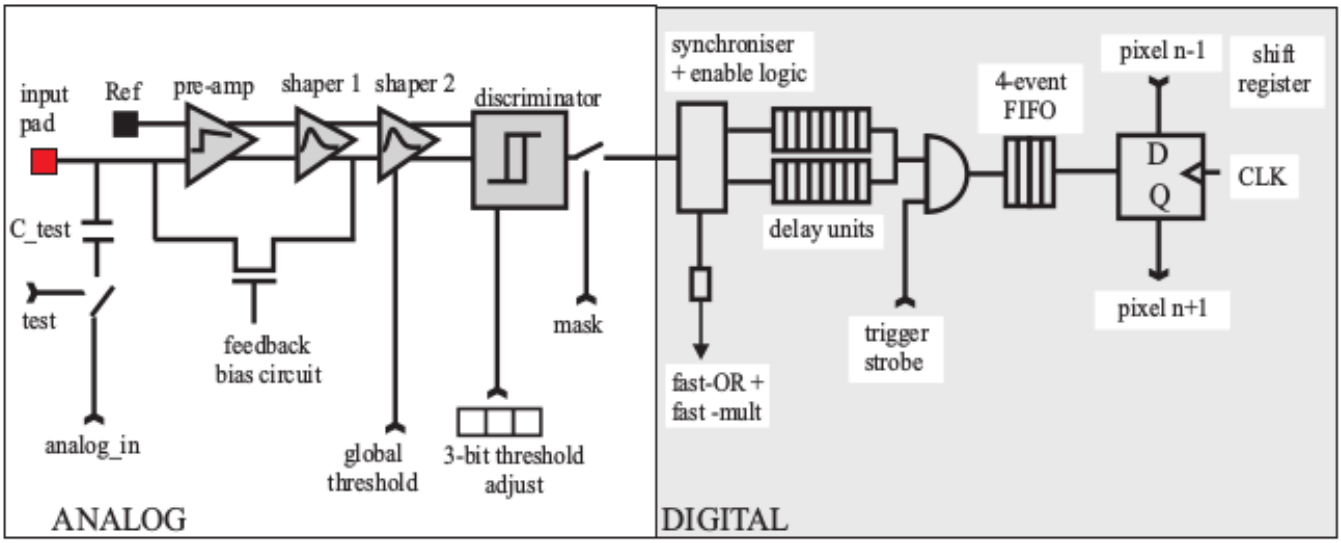

Figure 5: Schematic of the pixel cell [4, 5, 6].

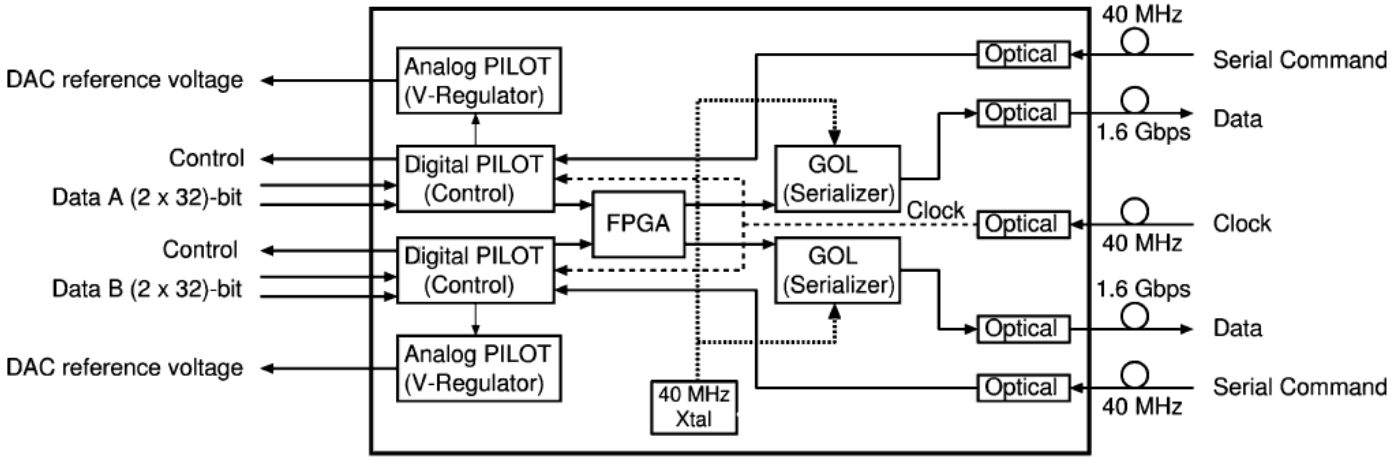

Figure 6: Brock diagram of SPIRO board.

hybrid. The radiation thickness requirements limit the number of layers that the bus can be resulting in a fine pitch bus design, i.e., $X/X_0 \sim 0.2\%$. Since fabrication of long (> 25 cm) fine pitch buses is difficult, the bus is split into two pieces. The fine pitch component that contains the sensor hybrids which we call the Pixel Bus, and an extender which we call the Bus Extender. The Pixel Bus is 13.9 mm wide and 250 mm long and is a Copper-Aluminum Polyimide FPC. The Bus Extender is outside the acceptance of the detector and is constructed using a wider pitch with more conventional Copper-Polymide FPC. The total length of the Pixel Bus is ~ 60 cm, as shown on Fig. 4.

2.1.5 Silicon Pixel Interface ReadOut (SPIRO) Board

The bus is connected to the Silicon Pixel Interface ReadOut (SPIRO) board which controls the readout chip and reads out and transfers the pixel data to the PHENIX DAQ system via 1.6 Gbit/sec optical links. Fig. 6 shows a block diagram of the SPIRO board which is designed to control two sensor hybrids independently. The SPIRO module has the following functions:

- Sending control information to the half ladder.
- Serializing the data from the half ladder and sending it to the **Front-End Module (FEM)** via optical links.

- Providing slow-control for pixel readout chips and the SPIRO board itself.
- Data format conversion to match PHENIX's DAQ requirement.

The primary component on the SPIRO board is the PHENIX Digital Pilot ASIC. Upon the pixel readout chip being initialized, each of the two pixel chip pairs present 256 × 2 sequential words of data on a 32-bit bus synchronously at the RHIC BCO frequency, 10 MHz, as shown in Figs. 3 and 6. Data is transmitted at 4 times the input frequency making four transmission cycles available before the next data word is received from the Pixel chips. This PHENIX pixel readout scheme has larger number of readout buses than the ALICE one to be able to use it in much higher trigger rates. However, the space budget for the SPIRO module is limited. Therefore, a modified PHENIX Digital Pilot ASIC with twice the number of input channel was developed. This ASIC uses the same design rules and radiation tolerant technology as the ALICE Pixel Pilot ASIC. It can handle 2 × 32 bit inputs which allows the simultaneous reading of two pixel chip words by one Digital Pilot ASIC. Each 32 bit input handles output from a pair of chips, which represent 512 sequential words of pixel data. Thus, two Digital Pilot ASICs are required to read data from 8 chips and it takes 51.2 μs to empty the pixel chips. A radiation hard ACTEL AX500-FGA484 receives the data from both PHENIX Digital Pilot chips, generates a check sum for each data stream, performs 8/10 bit encoding and provides time domain matching between the variable RHIC BCO clock frequency and the fixed GOL chip transmission frequency. Two analog pilot chips supply several reference voltages/currents, such as threshold voltages, and monitor for the ALICE Pixel chips on each sensor of the half ladder.

2.1.6 Front End Module (FEM)

The Pixel FEM is the interface between three SPIRO modules and the PHENIX DAQ and slow control systems. Since all communications with the SPIRO modules is by optical fiber, the Pixel FEM are located outside the radiation environment of the PHENIX experimental hall, eliminating the need for radiation tolerant components. Commands, initialization parameters, and clock timing information are transmitted to the SPIRO modules and pixel data is received from the SPIRO modules. This requires five optical fibers per SPIRO module. In order to allow simple manipulations of the data, the FEM pipes the data through an FPGA. This FPGA adds data headers and trailers to form standard PHENIX data packages. The design of the Pixel FEM is very similar by comparison to FEM's that are currently employed in the PHENIX readout system.

3 VTX Silicon Stripixel Tracker

The outer two barrels of the VTX detector for PHENIX experiment upgrade consists of silicon stripixel detector with a new "spiral" design, single-sided sensor with 2-dimensional (X-U) readout.

3.1 Novel Stripixel Sensor Design and Specifications

A novel stripixel silicon sensor has been developed at BNL. The silicon sensor is a single-sided, DC-coupled, two-dimensional (2D) sensitive detector. This design is simpler for sensor fabrication and signal processing than the conventional double-sided strip sensor. Each pixel from the stripixel sensor is made from two interleaved implants (a-pixel and b-pixel) in such a way that the charge deposited by ionizing particles can be seen by both implants as presented in figure **??**.A. The a-pixels are connected to form a X-strip as is presented in figure **??**.B. The b-pixels are connected in order to form a U-strip as is presented in figure **??**.C. The stereo angle between a X-strip and a U-strip is 4.6^o. A schematic cross section of the silicon stripixel sensor is presented in figure 8.a. The basic functionality of the sensor is simple; signal charges (electron−hole pairs) generated for example by particles produced from collisions are separated by the electric field, the electrons moving to the n^+ side, holes to the p^+ side, thus producing an electric

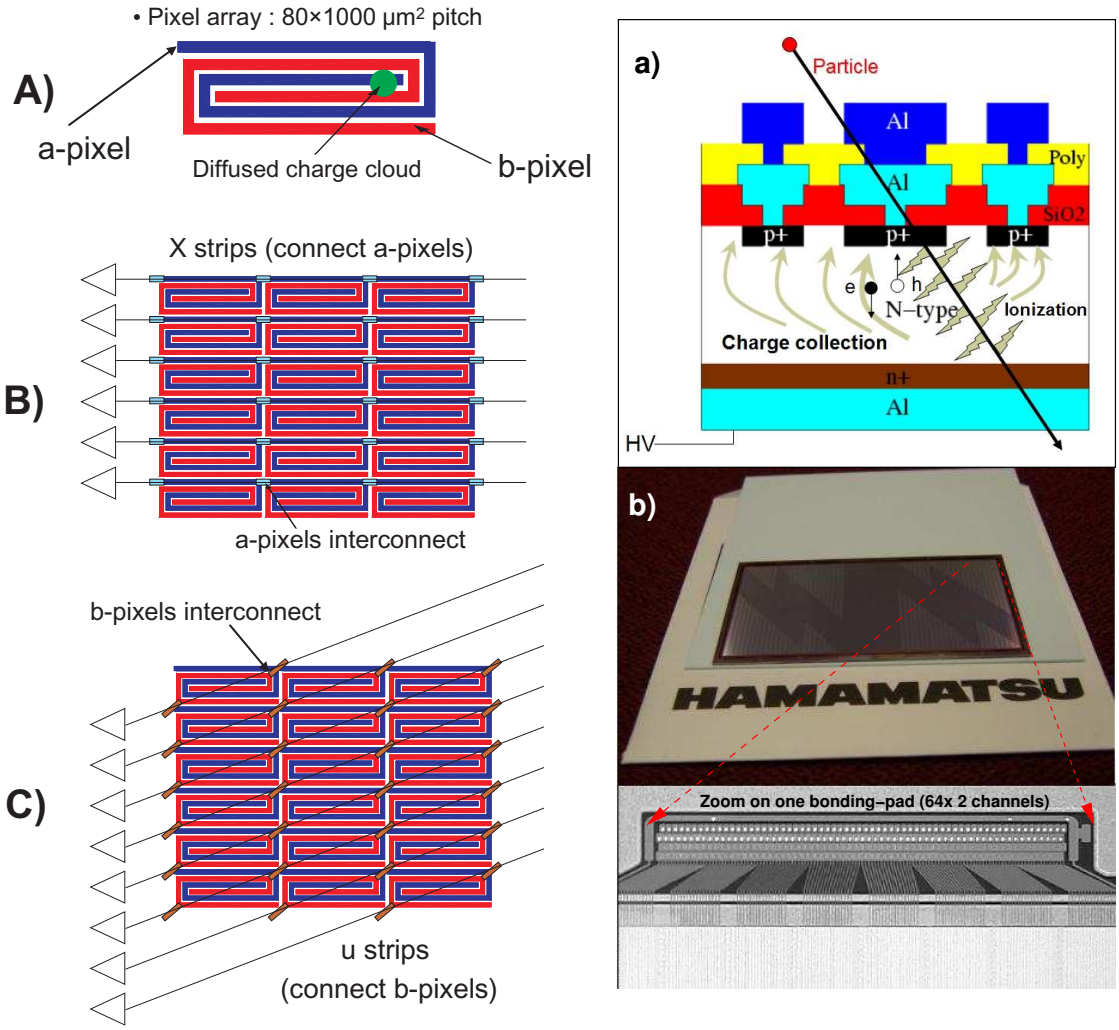

Figure 8: Panel a) Cross section view of double metal layout of silicon stripixel sensor via contacts on b-pixels of U-strip. Panel b) Photo of one silicon stripixel sensor from full-production fabricated by HPK.

signal which can be amplified and detected. In figure 8.a, the first Al layer is the metal contacts for all pixels. All X-strips are routed out by the first metal Al layer. All U-strips are routed out by the second metal Al layer.

The size of the silicon stripixel sensor is about 3.43×6.36 cm^2 and is shown in figure 8.b. In each long side of the sensor there are six sections of bonding pads, with 128 bonding pads each. This implies that each sensor has $2 \times 3 \times 128 = 768$ of X-strips of 80 μm width and 3.1 cm length in beam direction and the same number of U-strips at an angle of 4.6^o to the beam direction. Due to the stereoscopic readout the effective pixel size is 80×1000 μm. Five (for layer 3) or six (for layer 4) sensors are mounted in a ladder. The full length of a ladder in the beam direction is 31.8 cm (for layer 3) or 38.2 cm (for layer 4). A total of 44 ladders are required to cover the azimuth acceptance almost 2π. The geometric characteristics of silicon stripixel layers are presented in Table 1. The novel stripixel silicon sensor technology developed, including the mask design and processing technology, has been transferred from BNL to sensor fabrication company Hamamatsu Photonics (HPK) located in Japan, for mass production. A picture of one sensor from full production is presented in figure 8.b.

4 Performed Tests (Quality Assurance Tests)

In order to ensure correct operation of the silicon pixels detector, quality assurance (QA) test were performed on the pixels half ladder as well the electronics readout chain. As a reminder, the SPIRO board receives the data from half pixels ladder and sends it to the FEM via optical links. It should be noted that the SPIRO board provides all electrical power and control information to the sensor module and readout chip. The FEM receives the data from SPIRO board and send it to the PHENIX DAQ system. It also provides the clock, trigger and slow controls to the SPIRO board. To ensure best performance of half pixel ladder, the following QA tests were performed:

(1) **Current Consumption Test: (done in production QA and each pre-Run)**
The current consumption of the analog and digital circuits of the readout are measured. Good ladders to be used for the silicon pixel tracker must satisfy several criteria. One of the criteria is the current consumption of the readout chip. The consumption of an analog circuit of a chip must be smaller than 350 mA and that of a digital circuit must be smaller than 270 mA. The typical current consumption of the half ladder that consists of good readout chips results in 2.48 A with the power supply of 2.05 V. This corresponds to the power consumption of 1.3 W per chip and is consistent with the chip's design specification.

(2) **JTAG Functionality Test: (done in production QA)**
The test confirms whether the configuration settings in the chip can be controlled by using Joint Test Action Group (JTAG) protocol. Chips that failed the DAC setting via JTAG are excluded from the ladder production.

(3) **DAC Threshold (done in each pre-Run and during Run)**
The DAC threshold is determined as follows: First, noise data is taken before beam collisions by the so-called standalone mode where the DAC threshold is initially set at 170. Second, the DAC threshold is varied for a given chip so that the number of noise hits/chip/event is less than 10^{-4}. Third, any pixels that are excessively noisy pixels are masked. In addition to the DAC threshold determination prior the run, the DAC thresholds and pixel masks are interactively updated in beam collisions by monitoring the number of signal and noise hits/chip/event by online monitoring.

(4) **Pulse Test: (done in production QA and each pre-Run)**
Pulse tests are done to check for dead channels on each chip and for broken connection of the bump-bonding. The test pulse is transmitted 100 times from the pulsar into the chip to each pixel cell using a fixed patterns.

(5) **Test Using a β-ray source (^{90}Sr): (done in production QA)**
This aims to test the data taking ability of a given ladder with a self trigger. The self trigger uses the 'FastOR' that is issued by each chip. By the β-source measurements, faulty bump-bonds and the maximum efficiency are evaluated. Successful bump-bonding of more than 99 % is required for ladders used in the VTX pixel detector. This test has been done for each pixel ladder during the VTX pixels ladder production, see figure 9.

During QA test mentioned above, the bias voltage of the pixel ladders is set to 50 V to ensure best performance. During normal data taking the sensors are biased at 30-40 V.

4.1 Performance of Pixels Silicon Tracker in Run-16

4.1.1 Pre-Run (Physics Laboratory)

The VTX pixel detectors was tested in the PHENIX silicon laboratory at physics building at BNL prior to Run16. There, the following two types of tests were performed: **Tests (1) and (4)** described in Sec. 4.

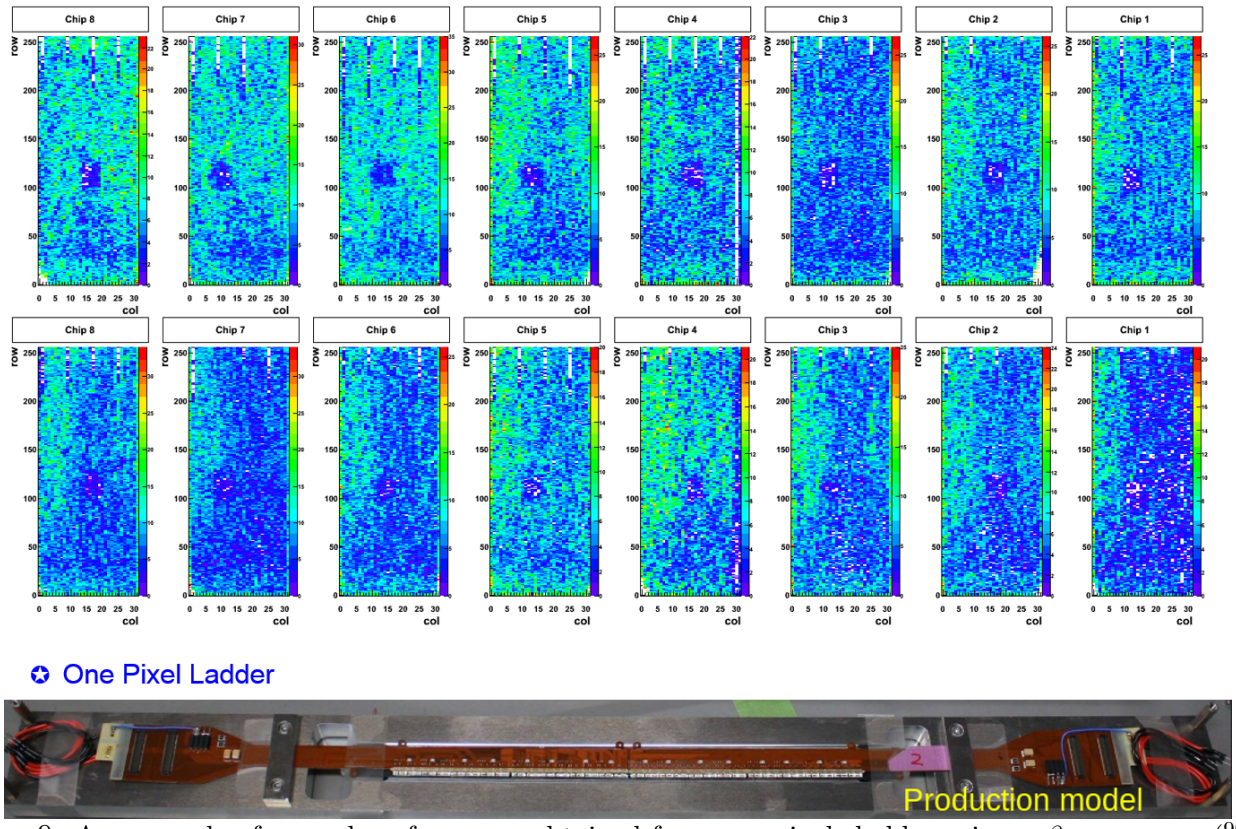

Figure 9: An example of a good performance obtained from one pixels ladder using a β-ray source (^{90}Sr).

Note that the FVTX detector was already installed onto the detector cage before performing these tests. For both B0 and B1, the pulse tests were performed on September 14, 2015 for West and on December 4, 2015 for East.

For Test (1), the current consumption of the analog and digital circuit of the readout chain are measured for all ladders prior to the pulse test which is described in the next paragraph. The power supplied to the ladder and SPIRO are about 3.5 V and 5.0 V, respectively. The currents are typically 4.0 A for ladder and 2.0 A for SPIRO, respectively. After the initialization of the chips and SPIRO, the currents decrease by 0.4 A for ladder and <0.02 A for SPIRO.

Figure 10 shows the power supplies used to power the FEM (left), ladder (right top), and SPIRO (right bottom). Bias voltage supply is located in the middle of Figure 10. Optical fibers from SPIRO are connected to FEM (bottom) and FEM is controlled by a desktop computer via 'OPS' software, a stand-alone software on a PC to communicate with a FEM and to test and to read-out a pixel ladder.

In Test (4), the bias voltage of 30 V is applied to ladders as a default to avoid the current going beyond 100 μA. For several ladders where the current would go beyond 100 μA at 30 V, we applied 15 V to those ladders. Note that bias voltages higher than 30 V are applied to some ladders during the data taking. The panel (a) and (b) in Fig. 11 show the results of the pulse test (namely Test (4) in Sec. 4) of the B0 West and B0 East layers, respectively. The panel (c) and (d) in Fig. 11 show the pulse test results of the B1 West and B1 East layers, respectively. Blank white spaces in the B1 layer indicate dead chips. In particular, both B1-L11 North and South are dead half ladders and thus fully dis-activated in Run16.

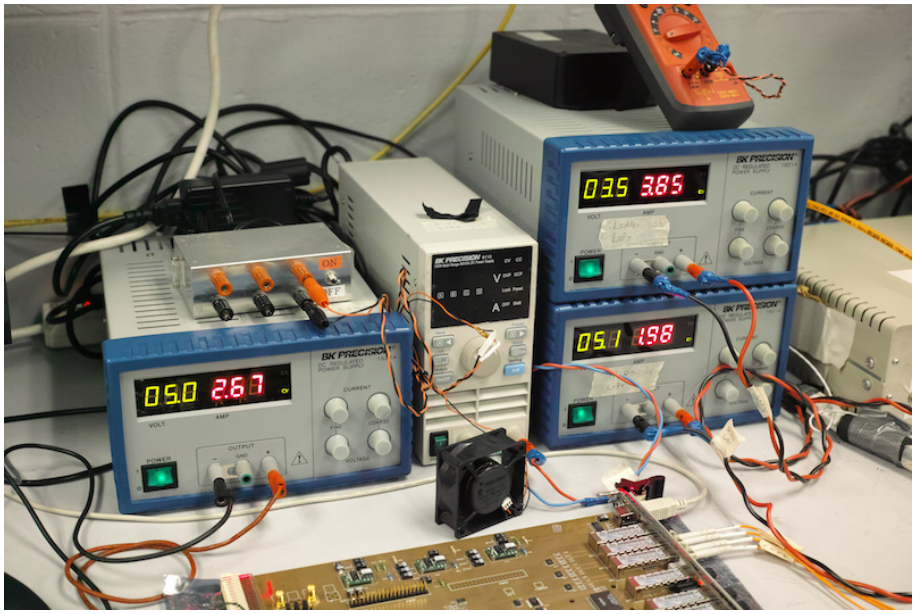

Figure 10: Layout of the pulse test bench and the current consumption measurement at physics laboratory prior to start Run.

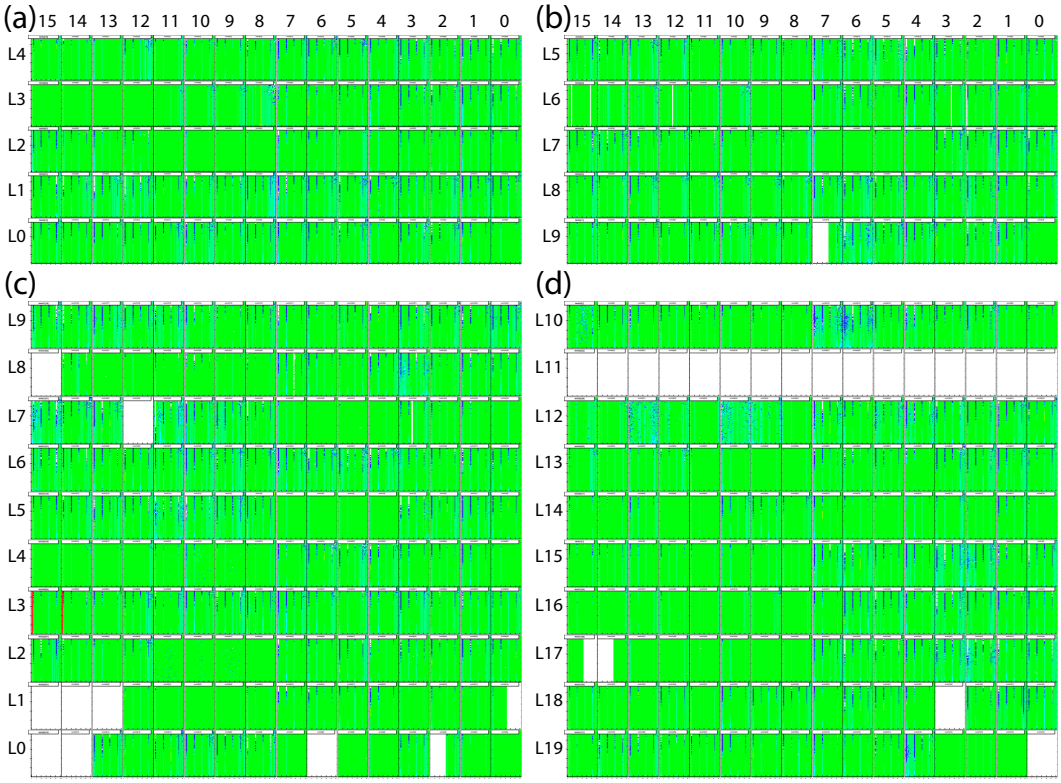

Figure 11: Pulse test results of B0 and B1 layers Pre-Run-16.

4.1.2 Over the Run (PHENIX IR)

The VTX pixel detector group has been monitoring the performance and operating parameters of the tracker since the beginning of Run16. Figure 12 indicates the percentage of live pixels for each chip in the B0 and B1 layers. Blue and red pixels indicate cold and hot pixels, respectively. A pixel that has a lower (higher) hit rate per event than the pre-defined criteria is recognized as a cold (hot) pixel. The criteria were determined at the beginning of Run16 by using a typical physics run. Unstable pixels (green) have a large fluctuation of the hit rate per event along the event sequence. Jump pixels (yellow) have sharp

B0 West			B0 Eest		
Ladder	Live area	Remark	Layer	Live area	Remark
L4	100 %		L5	100 %	
L3	100 %		L6	100 %	
L2	100 %		L7	100 %	
L1	100 %		L8	100 %	
L0	100 %		L9	97 %	Half chip dead in Run15
B1 West			B1 East		
Ladder	Live area	Remark	Layer	Live area	Remark
L9	100 %		L10	100 %	Chip 15 is unstable.
L8	94 %		L11	0 %	Fully dead since xxx.
L7	94 %		L12	100 %	
L6	100 %	North is unstable.	L13	100 %	
L5	100 %		L14	100 %	
L4	100 %		L15	100 %	
L3	100 %	Col. 0 is hot for chips 14 and 15	L16	100 %	
L2	100 %		L17	94 %	
L1	78 %		L18	94 %	
L0	78 %		L19	94 %	

Table 2: Quantitative Summary of the live area of B0 and B1 layers using Pulse Test Prior to Run-16.

descend or rise of the hit rate per event during run. Pixels filled by black color indicate the dead pixels. Good pixels (white) do not belong to any of the above categories. Thus the number of good pixels is obtained by subtracting the sum of the cold, hot, unstable, jump and dead (black) pixels from the number of all pixels. The number written down in each cell indicates the live area percentage that consists of only good pixels.

In the panel (a) and (b) of Fig. 12, there are jump pixels chips, shown as yellow chips. These instabilities may be caused by the event misalignment during data taking. As indicated in the panel (a) and (b), jump chips are distributed mainly in South East and North West. We have six and four jump chips in B0 West and East in Run 446864, respectively. These numbers vary run-by-run. Jump chips rarely appeared in the B1 layer as shown in the panel (c) and (d). Investigation into the understanding of the jump chip is ongoing. Note that the filled black area, corresponding to the dead pixels, are consistent with the location of dead chips measured by the Pulse Test prior to the start of Run16 (see Sec. 4.1.1). Live area percentage is summarized in Table 3, where the percentage consists of only good pixels. Once the jump chips are excluded from the live area percentages by event re-alignment, we obtain the improved live area percentage of B0 west and east as 88 % and 88 %, respectively. Live area percentages of the B1 layer do not significantly change, since jump chips rarely appeared in the B1 layer. Note that the live area in Table 3 is taken from Run 446864. The live area averaged over Run-16 may differ from those in Run 446864.

	West	East
B0	82 % (88 %)	84 % (88 %)
B1	72 %	69 %

Table 3: Summary of the live area percentages obtained in Au+Au at 200 GeV using Run 446864 (Run-16). For the B0 layer, the live area percentages that are corrected for jump chips are added in parentheses.

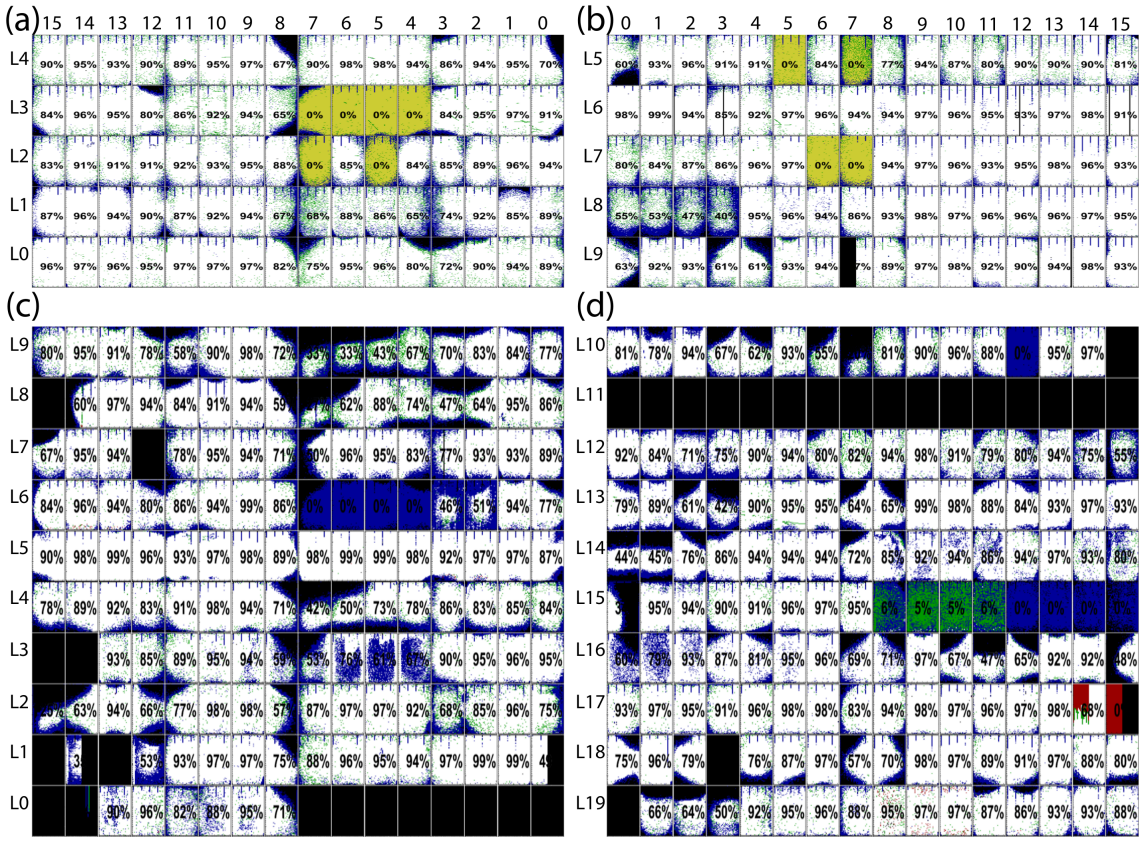

Figure 12: Data quality assurance from Run 446864 in Au+Au at 200 GeV (Run-16). Black point indicates a dead pixel. Red and blue points indicate hot and cold pixels, respectively. Green and yellow points indicate unstable and jump pixels, respectively. See text for more details.

4.2 Performance of Pixels Silicon Tracker in Run 15

4.2.1 Pre-Run (Physics Laboratory)

Test (1) was performed using the same method as described in Sec. 4.1.1. Almost same results were obtained by Test (1) as those at Pre-Run16, thus we omit describing the results in detail here.

Test (4) was also performed on November 2014 which was prior to Run15 in the same manner as for Run16. The panel (a) and (b) in Fig. 13 show the results of the pulse test of the B0 West and B0 East layers, respectively. The panel (c) and (d) in Fig. 13 show the pulse test results of the B1 West and B1 East layers, respectively. Blank white spaces in the B1 layer indicate the dead chips. Live area percentage for each ladder is summarized in Table 4.

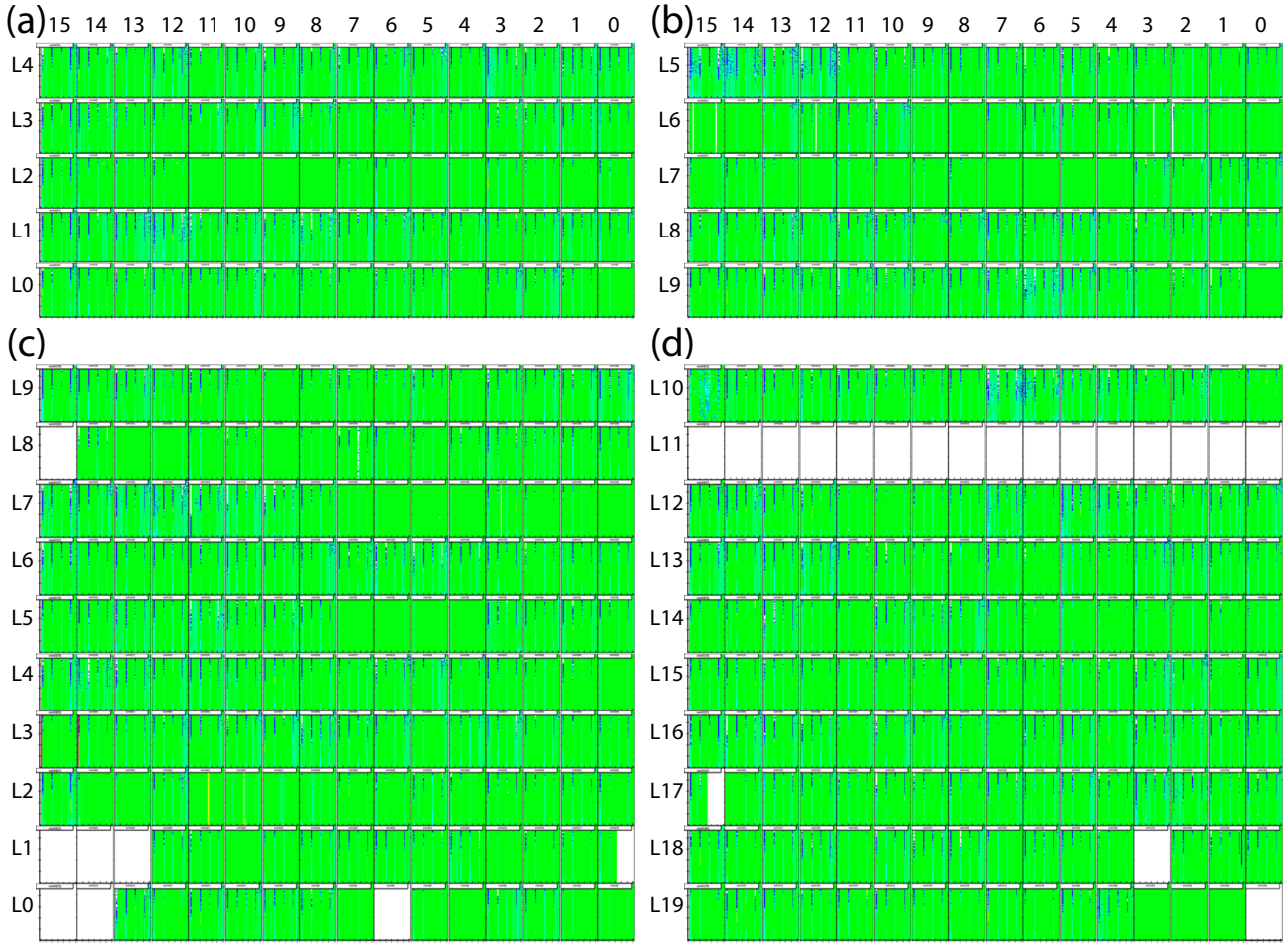

Figure 13: Pulse test results at Pre-Run15.

B0 West			B0 Eest		
ladder	Live area	Remark	Layer	Live area	Remark
L4	100 %		L5	100 %	
L3	100 %		L6	100 %	
L2	100 %		L7	100 %	
L1	100 %		L8	100 %	
L0	100 %		L9	100 %	
B1 West			B1 East		
Ladder	Live area	Remark	Layer	Live area	Remark
L9	100 %		L10	100 %	
L8	94 %		L11	0 %	Fully dead since xxx.
L7	100 %		L12	100 %	
L6	100 %	North is unstable.	L13	100 %	
L5	100 %		L14	100 %	
L4	100 %		L15	100 %	
L3	100 %	Col. 0 is hot for chips 14 and 15	L16	100 %	
L2	100 %		L17	97 %	
L1	78 %		L18	94 %	
L0	81 %		L19	94 %	

Table 4: Quantitative Summary of the live area of B0 and B1 layers using Pulse Test Prior to Run-15.

4.2.2 Over the Run (PHENIX IR)

During data taking of Run-15, one of the priorities of the VTX group is to monitor VTX (Pixels and Stripixels) detector. Figure 14 indicates the percentage of live area for each chip in the B0 and B1 layers. Pixels filled by white and black color indicate the good and dead pixels, respectively. Blue and red pixels indicate cold and hot ones, respectively. Unstable and jump pixels, no matter what the reason, are filled by green and yellow, respectively, although no significant number of jump or unstable pixels have been found in Figure 14 unlike in Run16. Definitions of good, dead, cold, hot, unstable, and jump pixels are presented in Sec. . The number written down in each cell of Figure 14 presents the live area percentage that consists of only good pixels. Note that the currently ongoing analyses indicate that a certain level of chips have suffered from the event misalignment that was mentioned in Sec. , thus the live area percentage may increase when event re-alignment is correctly performed. Live area percentage taken from Run 421716 is summarized in Table 5. The live area averaged over Run-15 differ within a few % from those in Run 421716 (p+p at 200 GeV).

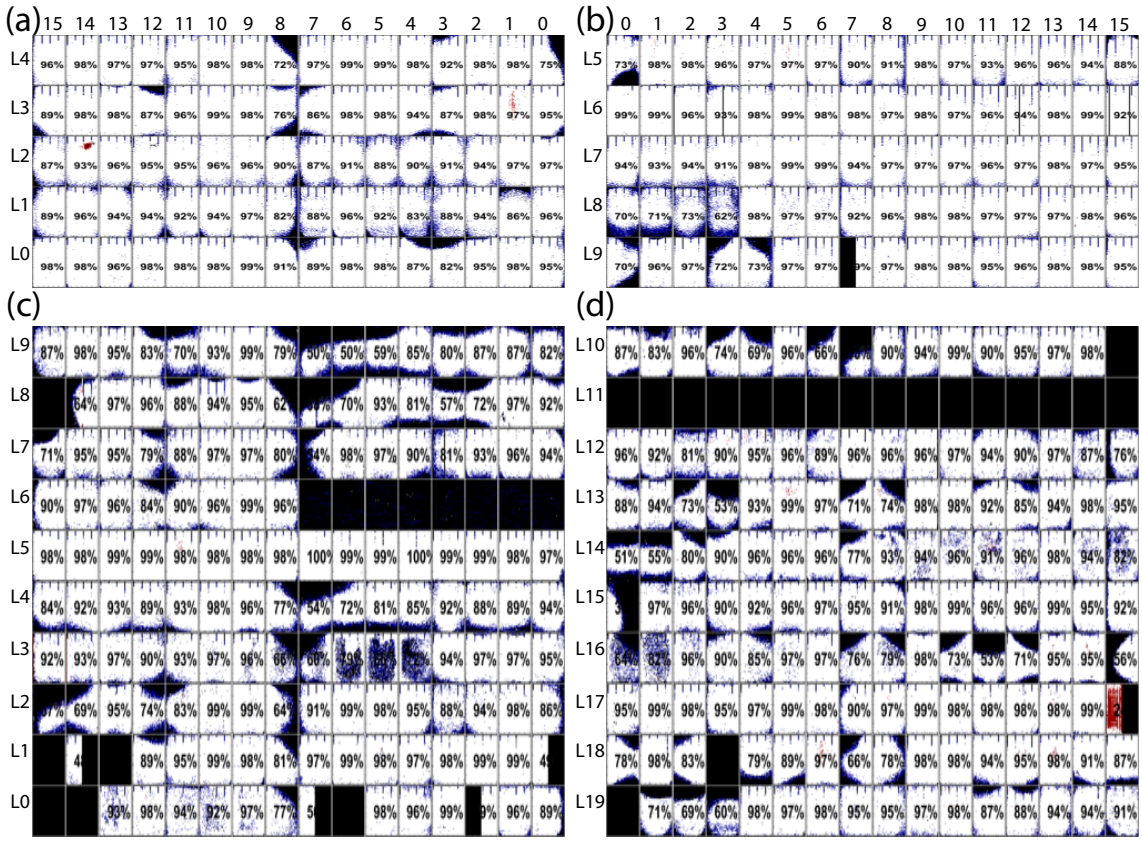

Figure 14: Data quality assurance from Run 421716 obtained in p+p collisions at 200 GeV (Run-15). Black point indicates a dead pixel. Red and blue points indicate hot and cold pixels, respectively. Green and yellow points indicate unstable and jump pixels, respectively. See text for more details.

	West	East
B0	93 %	93 %
B1	80 %	78 %

Table 5: Summary of the live area percentages obtained from Run 421716 in p+p collisions at 200 GeV (Run-15).

4.3 Performance of Pixels Silicon Tracker in Run 14

4.3.1 Over the Run (PHENIX IR)

During data taking of Run-14, the VTX experts were monitoring silicon pixels detector. Figure 15 shows the percentage of live area for each chip in the B0 and B1 layers. Pixels filled by white and black color indicate the good and dead pixels, respectively. Blue and red pixels indicate cold and hot ones, respectively. Unstable and jump pixels, no matter what the reason, are filled by green and yellow, respectively, although no significant number of jump or unstable pixels have been found in Figure 15 unlike in Run-16. Definitions of good, dead, cold, hot, unstable, and jump pixels are defined in Sec. . The number written down in each cell presents the live area percentage that consists of only good pixels. Note that the currently ongoing analyses indicate that a certain level of chips have suffered from the event misalignment that was mentioned in Sec. , thus the live area percentage may increase when event re-alignment is correctly performed. Live area percentage taken from Run 405860 is summarized in Table 6. The live area averaged over Run-14 differ within a few % from those from Run 405860 obtained in Au+Au at 200 GeV.

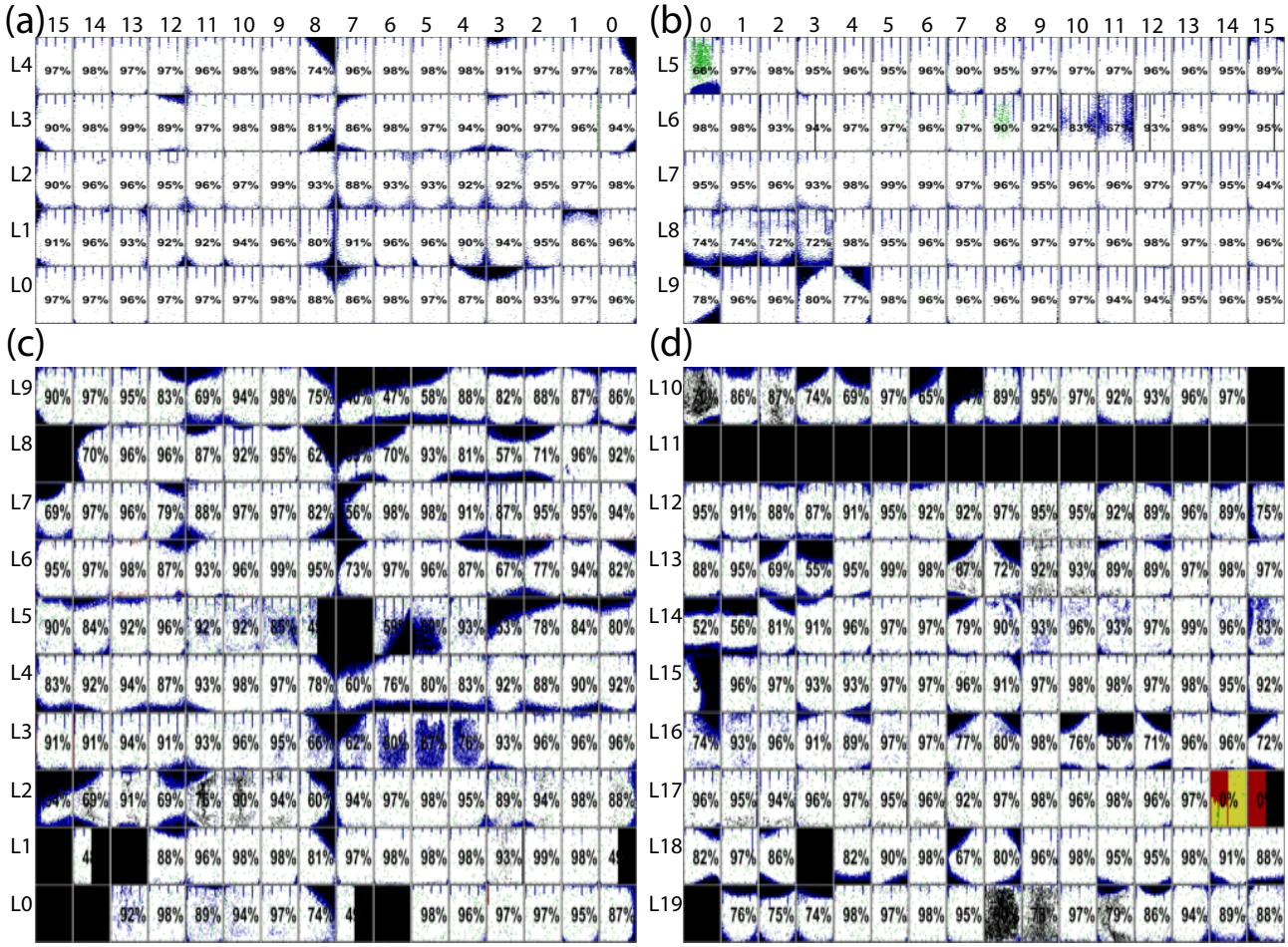

Figure 15: Data quality assurance in Run14 (Run 405860: Au+Au at 200 GeV).

	West	East
B0	94 %	93 %
B1	81 %	77 %

Table 6: Summary of the live area percentages obtained in Run 405860 from Au+Au at 200 GeV (Run-14).

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